AMENDMENTS TO THE CLAIMS

1. (currently amended) A datapath for processing input data, said datapath comprising:

at least one arithmetic pipeline, each pipeline inputting at least a portion of the input data and being controllable to perform at least one mathematical operation on the portion as it passes through the pipeline, each pipeline being capable of performing a four component dot product as the input data passes through said pipeline a single time,

wherein at least one pipeline is subdivided into a plurality of subsections, each subsection corresponding to a subset of the input data, and wherein at least one of said subsections comprises a flat four-input floating point adder module operating in parallel with floating point adders of other of said plurality of subsections.

2. (canceled)

3. (previously presented) The datapath of claim 1, wherein said at least one of said subsections further comprises:

a floating point multiplier module.

4. (previously presented) A datapath for processing input data, said datapath comprising:

at least one arithmetic pipeline, each pipeline inputting at least a portion of the input data and being controllable to perform at least one mathematical operation on the portion as it passes through the pipeline, each pipeline being capable of performing

a four component dot product as the input data passes through said pipeline a single time,

wherein at least one pipeline is subdivided into a plurality of subsections, each subsection corresponding to a subset of the input data, and wherein at least one of said subsections comprises a floating point multiplier module and a flat four-input floating point adder module, and

wherein said floating point multiplier module inputs the portion of the input data and performs a floating point multiply operation, and said flat four-input floating point adder module performs a normalization operation on a result of the floating point multiply operation.

5. (previously presented) A datapath for processing input data, said datapath comprising:

at least one arithmetic pipeline, each pipeline inputting at least a portion of the input data and being controllable to perform at least one mathematical operation on the portion as it passes through the pipeline, each pipeline being capable of performing a four component dot product as the input data passes through said pipeline a single time,

wherein at least one pipeline is subdivided into a plurality of subsections, each subsection corresponding to a subset of the input data, and wherein at least one of said subsections comprises a floating point multiplier module and a flat four-input floating point adder module, and

wherein said subsection further comprises a floating point-to-integer converter module controllable to convert a floating point number into one of a plurality of integer types and sizes.

6. (previously presented) The datapath of claim 1, wherein said plurality of subsections comprise:

a floating point multiplier module; and

a two-input floating point adder module.

7. (previously presented) A datapath for processing input data, said datapath comprising:

at least one arithmetic pipeline, each pipeline inputting at least a portion of the input data and being controllable to perform at least one mathematical operation on the portion as it passes through the pipeline, each pipeline being capable of performing a four component dot product as the input data passes through said pipeline a single time,

wherein at least one pipeline is subdivided into a plurality of subsections, each subsection corresponding to a subset of the input data, wherein said plurality of subsections comprise a floating point multiplier module and a two-input floating point adder module, and

wherein said floating point multiplier module inputs the portion of the input data and performs a floating point multiply operation, and said two-input floating point adder module performs a normalization operation on a result of the floating point multiply operation.

8. (original) The datapath of claim 1, wherein said at least one mathematical operation is a three component dot product that is performed as the input data passes through said pipeline a single time.

9. (currently amended) A processor executing arithmetic operations on vertex data, said processor comprising:

a data processing engine coupled to a first stage of said graphics pipeline, said processing engine comprising at least one arithmetic pipeline, each pipeline inputting at least a portion of the input data and being controllable to perform at least one mathematical operation on the portion as it passes through the pipeline, each pipeline being capable of performing a four component dot product as the input data passes through said pipeline a single time,

wherein at least one arithmetic pipeline is subdivided into a plurality of subsections, each subsection corresponding to a subset of the input data, and wherein at least one of said subsections comprises a flat four-input floating point adder module operating in parallel with floating point adders of other of said plurality of subsections.

10. (canceled)

11. (previously presented) The processor of claim 9, wherein said at least one of said subsections further comprises:

a floating point multiplier module.

12. (previously presented) A processor executing arithmetic operations on vertex data, said processor comprising:

a data processing engine coupled to a first stage of said graphics pipeline, said processing engine comprising at least one arithmetic pipeline, each pipeline inputting at least a portion of the input data and being controllable to perform at least one mathematical operation on the portion as it passes through the pipeline, each pipeline being capable of performing a four component dot product as the input data passes through said pipeline a single time,

wherein at least one arithmetic pipeline is subdivided into a plurality of subsections, each subsection corresponding to a subset of the input data, wherein at least one of said subsections comprises a floating point multiplier module and a flat four-input floating point adder module, and

wherein said floating point multiplier module inputs the portion of the input data and performs a floating point multiply operation, and said flat four-input floating point adder module performs a normalization operation on a result of the floating point multiply operation.

13. (previously presented) A processor executing arithmetic operations on vertex data, said processor comprising:

a data processing engine coupled to a first stage of said graphics pipeline, said processing engine comprising at least one arithmetic pipeline, each pipeline inputting at least a portion of the input data and being controllable to perform at least one mathematical operation on the portion as it passes through the pipeline, each pipeline being capable of performing a four component dot product as the input data passes through said pipeline a single time,

wherein at least one arithmetic pipeline is subdivided into a plurality of subsections, each subsection corresponding to a subset of the input data, wherein at

least one of said subsections comprises a floating point multiplier module and a flat four-input floating point adder module, and

wherein said subsection further comprises a floating point-to-integer converter module controllable to convert a floating point number into one of a plurality of integer types and sizes.

14. (previously presented) The processor of claim 9, wherein said plurality of subsections comprise:

a floating point multiplier module; and

a two-input floating point adder module.

15. (previously presented) A processor executing arithmetic operations on vertex data, said processor comprising:

a data processing engine coupled to a first stage of said graphics pipeline, said processing engine comprising at least one arithmetic pipeline, each pipeline inputting at least a portion of the input data and being controllable to perform at least one mathematical operation on the portion as it passes through the pipeline, each pipeline being capable of performing a four component dot product as the input data passes through said pipeline a single time,

wherein at least one arithmetic pipeline is subdivided into a plurality of subsections, each subsection corresponding to a subset of the input data, wherein said plurality of subsections comprise a floating point multiplier module and a two-input floating point adder module, and

wherein said floating point multiplier module inputs the portion of the input data and performs a floating point multiply operation, and said two-input floating point adder module performs a normalization operation on a result of the floating point multiply operation.

16. (original) The processor of claim 9, wherein said at least one mathematical operation is a three component dot product that is performed as the input data passes through said arithmetic pipeline a single time.

17. (currently amended) A graphics pipeline comprising:

a vertex engine coupled to a first stage of said graphics pipeline, said vertex engine comprising a plurality of datapaths, each datapath inputting vertex data and being controllable to perform at least one mathematical operation on the vertex data as the data passes through the datapath, wherein each datapath is capable of performing a three component dot product as the vertex data passes through said datapath a single time, and wherein a portion of the datapath comprises a flat four-input adder module operating in parallel with at least one floating point adder module of another portion of the datapath.

18. (original) The graphics pipeline of claim 17, wherein each datapath is capable of performing a four component dot product as the vertex data passes through said datapath a single time.

19. (original) The graphics pipeline of claim 17, wherein each datapath is a multi-function floating point pipeline.

Claims 20-31 (canceled)

32. (currently amended) A processor system comprising:

a processor; and

a data processing pipeline coupled to said processor, said data processing pipeline comprising at least one datapath, each datapath inputting data and being controllable to perform at least one mathematical operation on the data as the data passes through the datapath, wherein each datapath is capable of performing a four component dot product as the data passes through said datapath a single time, and wherein a portion of the datapath comprises a flat four-input adder module operating in parallel with at least one floating point adder module of another portion of the datapath.

33. (currently amended) A processor system comprising:

a processor; and

a graphics point pipeline coupled to said processor, said graphics pipeline comprising a vertex engine coupled to a first stage of said pipeline, said vertex engine comprising a plurality of datapaths, each datapath inputting vertex data and being controllable to perform at least one mathematical operation on the vertex data as the data passes through the datapath, wherein each datapath is capable of performing a three component dot product as the vertex data passes through said datapath a single time, and wherein a portion of the datapath comprises a flat four-input adder module operating in parallel with at least one floating point adder module of another portion of the datapath.

34. (original) The system of claim 33, wherein each datapath is capable of performing a four component dot product as the vertex data passes through said datapath a single time.